DPN+RPN
equivalent?

DOCUMENT-IDENTIFIER: US 20020185675 A1

TITLE: SOI device with reduced junction capacitance

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[0025] Referring to the drawings, FIGS. 3A through 3E are partial cross-sectional views illustrating the fabrication of an SOI FET device according to a first embodiment of the present invention. The fabrication method starts in FIG. 3A, with a silicon substrate 300 having a BOX 305 formed between a thin silicon layer 310 and the substrate. Extending from a top surface 315 of silicon layer 310, through the silicon layer, to BOX 305 is STI 320. STI 320 may be formed by a photolithographic step, followed by a reactive ion etch (RIE) of silicon substrate 300 to form a trench down to BOX 305, followed by deposition of an insulator to fill the trench so formed, followed by a chemical-mechanical-polish (CMP) process to planarize to form top surface 315. In one example, BOX 305 is formed by ion implantation of oxygen and comprises silicon oxide about 50 to 500 . . . in thickness, and silicon layer 310 is 50 to 500 . . . in thickness being either P or N doped to about 10.sup.16 to 10.sup.18 atm/cm.sup.3. Formed on top of top surface 315 is a gate dielectric 325. In one example, gate dielectric 325 is silicon dioxide is

formed by thermal oxidation or chemical vapor deposition (CVD) and is about 10 . . . to 50 . . . in thickness. In another example, gate dielectric 325 is silicon oxynitride formed by thermal oxidation followed by nitridation of the oxide by remote plasma nitration (RPN) or decoupled plasma nitridation (DPN.) In still another example, gate dielectric 325 is a high-K material such as aluminum oxide or hafnium oxide formed by CVD. Formed on top of gate dielectric 325 is gate conductor 330 and formed on top of the gate conductor is hard mask 335. In one example, gate conductor 330 is polysilicon formed by CVD and is about 500 . . . to 2000 . . . in thickness and hard mask 335 is silicon oxide, formed by oxidation or CVD, silicon nitride, formed by CVD or a combination thereof, and is 100 . . . to 1000 . . . in thickness. Hard mask 335 is used to prevent subsequent ion implantation processes, as illustrated in FIG. 3D, and described below from penetrating into gate conductor 330 or gate dielectric 325. Formed on hard mask 335 is photoresist 340. Photoresist 340 is patterned with an FET gate pattern and is aligned over silicon layer 310 between STI 320.

DPN + RPN
equivalents

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TITLE: Method of forming low-leakage on-chip capacitor

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An improved capacitor is formed by a process where an improved node dielectric layer is formed with an improved dielectric constant by performing an Free Radical Enhanced Rapid Thermal Oxidation (FRE RTO) step during formation of the node dielectric layer. Use of an FRE RTO step instead of the conventional furnace oxidation step produces a cleaner oxide with a higher dielectric constant and higher capacitance. Other specific embodiments of the invention include improved node dielectric layer by one or more additional nitridation steps, done by either Remote Plasma Nitridation (RPN), Rapid Thermal Nitridation (RTN), Decoupled Plasma Nitridation (DPN) or other nitridation method; selective oxidation; use of a metal layer rather than a SiN layer as the dielectric base; and selective oxidation of the metal layer.

The present invention provides an improved node dielectric layer for an on-chip capacitor and method of fabricating the layer which increases its performance. In particular, the present invention

includes a Free Radical
Enhanced Rapid Thermal Oxidation (FRE RTO) step
while forming the node
dielectric layer of an on-chip capacitor instead of
a furnace oxidation step to
produce a cleaner oxide than the furnace oxide.
The cleaner oxide formed by
the FRE RTO step results in a higher energy barrier
between the electrodes and
the node dielectric layer which results in lower
leakage and higher
performance. Other specific embodiments of the
invention include: a Low
Pressure Chemical Yapor Deposition (LPCVD) of SiN
step; a nitridation step,
done by either Remote Plasma Nitridation (RPN),
Rapid Thermal Nitridation
(RTN), Decoupled Plasma Nitridation (DPN) or other
nitridation method;
selective oxidation; deposition of a metal layer;
and selective oxidation of
the metal layer. Combinations of these various
process steps of forming a node
dielectric layer improve the layer quality and,
thus, the performance of the
node dielectric layer. The improved dielectric
layer, therefore, increases the
capacitance of the on-chip capacitor without a
substantial increase in the
leakage current. Alternatively, the improved
dielectric layer decreases the
leakage without a decrease in the capacitance.

2. The method of claim 1, wherein the step of
forming said nitride film
comprises nitriding at least a portion of the
additional nitride by at least
one method selected from remote plasma nitridation
rapid thermal nitridation
and decoupled plasma nitridation.

3. The method of claim 1, further comprising nitriding at least a portion of the oxidized portion of the nitride film by at least one method selected from remote plasma nitridation, rapid thermal nitridation and decoupled plasma nitridation.